a memory coupled to said processing unit and capable of storing information provided by said processing unit, said memory occupying a larger area of said integrated circuit substrate than said processing unit said memory further occupying a majority of a total area of said single substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

5. (amended) The microprocessor integrated circuit of claim 4 wherein said memory is dynamic random-access memory.

6. (amended) The microprocessor integrated circuit of claim 4 wherein said memory is static random-access memory.

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7. (amended) The microprocessor integrated circuit of claim 4 wherein said memory is capable of supporting read and write operations.

8. (amended) A microprocessor integrated circuit comprising:

a processing unit having one or more interface ports for interprocessor communication, said processing unit being disposed on a single substrate;

a memory disposed upon said substrate and coupled to said processing unit, said memory occupying a greater area of said substrate than said processing unit, said memory further comprising a majority of a total area of said substrate; and

a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said substrate.

9. (amended) The microprocessor integrated circuit of claim 8 wherein a first of said interface ports includes a column latch, said column latch facilitating serial communication through said first of said interface ports.



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